

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/96

Serial No.  
10/551891

Applicant(s)  
Vorbach et al.

Filing Date  
August 28, 2006

Group Art Unit  
2125

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	2005/0144215	Jun 30, 2005	Simkins et al.			
	2005/066213	March 2005	Vorbach et al.			
	2006/0230094	Oct 12, 2006	Simkins et al.			
	2006/0130096	Oct 12, 2006	Thendean et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 746 106	December 4, 1996	EPO				
	1 061 439	December 20, 2000	EPO				
	1 669 885	Jun 14, 2006	EPO			Abstract	
	WO98/10517	March 12, 1998	PCT				
	WO98/35294	August 13, 1998	PCT				
	WO00/49496	August 24, 2000	PCT				
	WO02/50665	June 27, 2002	PCT				
	WO 2004/053718	June 24, 2004	PCT				
	WO05/045692	May 19, 2005	PCT				
	05-509184	December 16, 2003	Japan			English Equivalent = USP 5,193,202 cited above	
	08069447	March 12, 1996	Japan			Abstract	
	2001-500682	January 16, 2001	Japan			Abstract	
	2000-201066	July 18, 2000	Japan			Abstract	

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Abnous et al., "Ultra-Low-Power Domain-Specific Multimedia Processors," U.C. Berkeley, 1996 IEEE, pp. 461-470.
	Albaharna, O.T. et al., "On the Viability of FPGA-Based Integrated Coprocessors," Dept. of Electrical and Electronic Engineering, Imperial College of Science, London, 1999 IEEE, pp. 206-215.
	Altera, "Flex 8000 Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-62.
	Altera, "Flex 10K Embedded Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-128.
	Atmel, 5-K-50K Gates Coprocessor FPGA with Free Ram, Data Sheet, July 2006, 55 pages.
	Atmel, FPGA-based FIR Filter Application Note, September 1999, 10 pages.
	Atmel, "An Introduction to DSP Applications using the AT40K FPGA," FPGA Application Engineering, San Jose, CA, April 2004, 15 pages.
	Atmel, Configurable Logic Design & Application Book, Atmel Corporation, 1995, pp. 2-19 through 2-25.

The PTO did not receive the following listed item(s) All "for" document,



**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/96

Serial No.  
10/551891

Applicant(s)  
Vorbach et al.

Filing Date  
August 28, 2006

Group Art Unit  
2125

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE37,195	May 29, 2001	Kean			
	4,590,583	May 20, 1986	Miller			
	4,667,190	May 1987	Fant et al.			
	4,972,314	November 1990	Getzinger et al.			
	5,010,401	April 1991	Murakami et al.			
	5,034,914	July 1991	Osterlund			
	5,041,924	August 1991	Blackborow et al.			
	5,065,308	November 12, 1991	Evans			
	5,099,447	March 1992	Myszewski			
	5,237,686	August 1993	Asano et al.			
	5,276,836	January 4, 1994	Fukumaru et al.			
	5,327,125	July 1994	Iwase et al.			
	5,343,406	Aug 30, 1994	Freeman et al.			
	5,418,953	May 1995	Hunt et al.			
	5,469,003	November 1995	Kean			
	5,537,580	July 1996	Giomi et al.			
	5,550,782	Aug 27, 1996	Cliff et al.			
	5,625,836	Apr 29, 1997	Barker et al.			
	5,646,544	Jul 8, 1997	Iadanza			
	5,646,545	Jul 8, 1997	Trimberger et al.			
	5,581,731	December 3, 1996	King et al.			
	5,737,565	April 1998	Mayfield			
	5,754,459	May 19, 1998	Telikepalli			
	5,754,820	May 19, 1998	Yamagami			
	5,781,756	Jul 14, 1998	Hung			
	5,781,756	Jul 14, 1998	Hung			
	5,801,958	September 1998	Dangelo et al.			
	5,815,715	September 1998	Kayhan			
	5,831,448	Nov 3, 1998	Kean			
	5,844,422	December 1, 1998	Trimberger et al.			
	5,857,097	January 1999	Henzinger et al.			
	5,862,403	January 1999	Kanai et al.			
	5,870,620	Feb 9, 1999	Kadosumi et al.			
	5,889,533	Mar 30, 1999	Lee			
	5,933,023	Aug 3, 1999	Young			
	5,960,193	September 28, 1999	Guttag et al.			
	5,966,143	Oct 12, 1999	Breternitz, Jr.			
	5,978,583	November 1999	Ekanadham et al.			

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/96

Serial No.  
10/551891

Applicant(s)  
Vorbach et al.

Filing Date  
August 28, 2006

Group Art Unit  
2125

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,999,990	December 1999	Sharrit et al.			
	6,020,760	February 1, 2000	Sample et al.			
	6,044,030	Mar 28, 2000	Zheng et al.			
	6,077,315	June 2000	Greenbaum et al.			
	6,084,429	July 2000	Trimberger			
	6,105,106	August 2000	Manning			
	6,134,166	October 17, 2000	Lytle et al.			
	6,137,307	October 2000	Iwanczuk et al.			
	6,154,048	November 2000	Iwanczuk et al.			
	6,154,049	Nov 28, 2000	New			
	6,157,214	December 5, 2000	Marshall			
	6,185,256	February 2001	Saito et al.			
	6,185,731	February 2001	Maeda et al.			
	6,198,304	March 2001	Sasaki			
	6,201,406	March 2001	Iwanczuk et al.			
	6,204,687	March 2001	Schultz et al.			
	6,215,326	April 10, 2001	Jefferson et al.			
	6,216,223	April 2001	Revilla et al.			
	6,252,792	June 26, 2001	Marshall et al.			
	6,262,908	July 17, 2001	Marshall et al.			
	6,266,760	July 2001	DeHon et al.			
	6,285,624	September 2001	Chen			
	6,311,265	October 2001	Beckerle et al.			
	6,353,841	March 5, 2002	Marshall et al.			
	6,362,650	Mar 26, 2002	New et al.			
	6,373,779	Apr 16, 2002	Pang et al.			
	6,381,624	April 2002	Colon-Bonet et al.			
	6,400,601	June 2002	Sudo et al.			
	6,421,808	July 2002	McGeer			
	6,427,156	Jul 30, 2002	Chapman et al.			
	6,430,309	August 2002	Pressman et al.			
	6,434,642	Aug 13, 2002	Camilleri et al.			
	6,438,747	August 2002	Schreiber et al.			
	6,477,643	November 5, 2002	Vorbach et al.			
	6,487,709	November 2002	Keller et al.			
	6,507,947	January 2003	Schreiber et al.			
	6,516,382	February 2003	Manning			
	6,518,787	February 2003	Allegrucci et al.			

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/96

Serial No.  
10/551891

Applicant(s)  
Vorbach et al.

Filing Date  
August 28, 2006

Group Art Unit  
2125

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,523,107	February 18, 2003	Stansfield et al.			
	6,525,678	February 2003	Veenstra et al.			
	6,539,415	March 25, 2003	Mercs			
	6,539,438	March 25, 2003	Ledzius et al.			
	6,542,394	April 1, 2003	Marshall et al.			
	6,553,395	April 22, 2003	Marshall et al.			
	6,567,834	May 20, 2003	Marshall et al.			
	6,631,487	October 2003	Abramovici et al.			
	6,708,325	March 2004	Cooke et al.			
	6,721,830	April 2004	Vorbach et al.			
	6,754,805	June 2004	Yujen Juan			
	6,757,892	June 2004	Gokhale et al.			
	6,782,445	August 2004	Olgiati et al.			
	6,802,206	October 2004	Patterson et al.			
	6,820,188	November 16, 2004	Stansfield et al.			
	6,829,697	December 2004	Davis et al.			
	6,847,370	January 2005	Baldwin et al.			
	6,871,341	March 2005	Shyr			
	6,874,108	March 2005	Abramovici et al.			
	6,977,649	December 2005	Baldwin et al.			
	7,007,096	February 2006	Lisitsa et al.			
	7,010,687	March 2006	Ichimura			
	7,038,952	May 2, 2006	Zack et al.			
	7,210,129	April 2007	May et al.			
	7,237,087	June 26, 2007	Vorbach et al.			
	7,249,351	July 2007	Songer et al.			
	7,254,649	August 2007	Subramanian et al.			
	7,350,178	March 2008	Crosland et al.			
	2001/001860	May 2001	Bieu			
	2002/124238	September 05, 2002	Metzgen			
	2003/061542	March 2003	Bates et al.			
	2003/062922	Apr 3, 2003	Douglass et al.			
	2005/0144210	Jun 30, 2005	Simkins et al.			
	2005/0144212	Jun 30, 2005	Simkins et al.			

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/96

Serial No.  
10/551891

Applicant(s)  
Vorbach et al.

Filing Date  
August 28, 2006

Group Art Unit  
2125

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Atmel, Field Programmable Gate Array Configuration Guide, AT6000 Series Configuration Data Sheet, September 1999, pp. 1-20.
	Athanasis et al., "Processor Reconfiguration Through Instruction-Set Metamorphosis," 1993, IEEE Computers, pp. 11-18.
	Bakkes, P.J., et al., "Mixing Fixed and Reconfigurable Logic for Array Processing," Dept. of Electrical and Electronic Engineering, University of Stellenbosch, South Africa, 1996 IEEE, pp. 118-125.
	Bacon, D. et al., "Compiler Transformations for High-Performance Computing," ACM Computing Surveys, 26(4):325-420 (1994)
	Becker, J. et al., "Architecture, Memory and Interface Technology Integration of an Industrial/Academic Configurable System-on-Chip (CSoC)," IEEE Computer Society Annual Workshop on VLSI (WVLSI 2003), (February 2003)
	Becker, J., "Configurable Systems-on-Chip (CSoC)," (Invited Tutorial), Proc. of 9th Proc. of XV Brazilian Symposium on Integrated Circuit, Design (SBCCI 2002), (September 2002)
	Becker et al., "Automatic Parallelism Exploitation for FPL-Based Accelerators." 1998, Proc. 31 <sup>st</sup> Annual Hawaii International Conference on System Sciences, pp. 169-178.
	Bratt, A, "Motorola field programmable analogue arrays, present hardware and future trends," Motorola Programmable Technology Centre, Gadbrook Business Centre, Northwich, Cheshire, 1998, The Institute of Electrical Engineers, IEE, Savoy Place, London, pp. 1-5.
	Cardoso, J.M.P. et al., "A novel algorithm combining temporal partitioning and sharing of functional units," University of Algarve, Faro, Portugal, 2001 IEEE, pp. 1-10.
	Cardoso, J.M.P. et al., "Compilation and Temporal Partitioning for a Coarse-Grain Reconfigurable Architecture," LYSACHT, P. & ROSENTIEL, W. eds., "New Algorithms, Architectures and Applications for Reconfigurable Computing," (2005) pp. 105-115
	Cardoso, J.M.P. et al., "Macro-Based Hardware Compilation of Java <sup>TM</sup> Bytecodes into a Dynamic Reconfigurable Computing System," Field-Programmable Custom Computing Machines (1999) FCCM '99. Proceedings. Seventh Annual IEEE Symposium on NAPA Valley, CA, USA, 21-23 April 1999, IEEE Comput. Soc, US, (21 April 1999) pp.2-11
	Compton, K. et al., "Configurable Computing: A Survey of Systems and Software," Northwestern University, Dept. of ECE, Technical Report, 1999, (XP-002315148), 39 pages.
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0702, 2007, pp. 1-15, <a href="http://www.clearspeed.com">www.clearspeed.com</a> .
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0306, 2006, pp. 1-14, <a href="http://www.clearspeed.com">www.clearspeed.com</a> .
	Cook, Jeffrey J., "The Amalgam Compiler Infrastructure," Thesis at the University of Illinois at Urbana-Champaign (2004) Chapter 7 & Appendix G
	Cronquist, D. et al., 'Architecture Design of Reconfigurable Pipelined Datapaths,' Department of Computer Science and Engineering, University of Washington, Seattle, WA, Proceedings of the 20 <sup>th</sup> Anniversary Conference on Advanced Research in VSLI, 1999, pp. 1-15.
	DeHon, Andre, "Reconfigurable Architectures for General-Purpose Computing," Massachusetts Institute of Technology, Technical Report AIRTR-1586, October 1996 (1996-10), XP002445054, Cambridge, MA, pp. 1-353.
	Diniz, P., et al., "A behavioral synthesis estimation interface for configurable computing," University of Southern California, Marina Del Rey, CA, 2001 IEEE, pp. 1-2.
	Ebeling, C. et al., "Mapping Applications to the RaPiD Configurable Architecture," Department of Computer Science and Engineering, University of Washington, Seattle, WA, <u>FPGAs for Custom Computing Machines</u> , 1997. Proceedings., The 5th Annual IEEE Symposium, Publication Date: 16-18 Apr 1997, 10 pages.
	Equator, Pixels to Packets, Enabling Multi-Format High Definition Video, Equator Technologies BSP-15 Product Brief, <a href="http://www.equator.com">www.equator.com</a> , 2001, 4 pages.
	Fawcett, B.K., "Map, Place and Route: The Key to High-Density PLD Implementation," Wescon Conference, IEEE Center (7 November 1995) pp. 292-297
	Freescale Slide Presentation, An Introduction to Motorola's RCF (Reconfigurable Compute Fabric) Technology, Presented by Frank David, Launched by Freescale Semiconductor, Inc., 2004, 39 pages.
	Genius, D. et al., "A Case for Array Merging in Memory Hierarchies," Proceedings of the 9th International Workshop on Compilers for Parallel Computers, CPC'01 (June 2001), 10 pages.
	Hartenstein, R. et al., "A new FPGA architecture for word-oriented datapaths," Proc. FPL'94, Springer LNCS, September 1994, pp. 144-155.
	Hendrich, N., et al., "Silicon Compilation and Rapid Prototyping of Microprogrammed VLSI-Circuits with MIMOLA and SOLO 1400," Micropocessing & Microprogramming (September 1992) vol.35(1-5), pp. 287-294

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/96

Serial No.  
10/551891

Applicant(s)  
Vorbach et al.

Filing Date  
August 28, 2006

Group Art Unit  
2125

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Hwang, K., "Advanced Computer Architecture – Parallelism, Scalability, Programmability," 1993, McGraw-Hill, Inc., pp. 348-355.
	Hwang, K., "Computer Architecture and Parallel Processing," Data Flow Computers and VLSI Computations, XP-002418655, 1985 McGraw-Hill, Chapter 10, pp. 732-807.
	IBM Technical Disclosure Bulletin, IBM Corp., New York, XP000424878, Bd. 36, Nr. 11, 1 November 1993, pp. 335-336.
	Inside DSP, "Ambric Discloses Massively Parallel Architecture," August 23, 2006, <a href="HTTP://insidedsp.com/tabcid/64/articleType/ArticleView/articleId/155/Defa...">HTTP://insidedsp.com/tabcid/64/articleType/ArticleView/articleId/155/Defa...</a> , 2 pages.
	Intel, Intel MXP5800/MXP5400 Digital Media Processors, Architecture Overview, June 2004, Revision 2.4, pp. 1-14.
	Kaul, M., et al., "An automated temporal partitioning and loop fission approach of FPGA based reconfigurable synthesis of DSP applications," University of Cincinnati, Cincinnati, OH, ACM 1999, pp. 616-622.
	Kean, T.A., "Configurable Logic: A Dynamically Programmable Cellular Architecture and its VLSI Implementation," University of Edinburgh (Dissertation) 1988, pp. 1-286
	Kean, T., et al., "A Fast Constant Coefficient Multiplier for the XC6200," Xilinx, Inc., Lecture Notes in Computer Science, Vol. 1142, Proceedings of the 6 <sup>th</sup> International Workshop of Field-Programmable Logic, 1996, 7 pages.
	Kim et al., "A Reconfigurable Multifunction Computing Cache Architecture," IEEE Transactions on Very Large Scale Integration (VLSI) Systems Volume 9, Issue 4, Aug 2001 Page(s):509 – 523.
	Knittel, Gunter, "A PCI-compatible FPGA-Coprocessor for 2D/3D Image Processing," University of Turgingen, Germany, 1996 IEEE, pp. 136-145.
	Koch, Andreas et al., "High-Level-Language Compilation for Reconfigurable Computers," Proceedings of European Workshop on Reconfigurable Communication-Centric SOCS (June 2005) 8 pages
	Larsen, S. et al., "Increasing and Detecting Memory Address Congruence," Proceedings of the 2002 IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'02), pp. 1-12 (September 2002).
	Lee et al., "A new distribution network based on controlled switching elements and its applications," IEEE/ACT Trans. of Networking, Vol. 3, No. 1, pp. 70-81, February 1995.
	Margolus, N., "An FPGA architecture for DRAM-based systolic computations," Boston University Center for Computational Science and MIT Artificial Intelligence Laboratory, IEEE 1997, pp. 2-11.
	Mei, Bingfeng, "A Coarse-Grained Reconfigurable Architecture Template and Its Compilation Techniques," Katholieke Universiteit Leuven, PhD Thesis, January 2005, IMEC vzw, Universitair Micro-Electronica Centrum, Belgium, pp. 1-195 (and Table of Contents).
	Mei, Bingfeng, et al., "Design and Optimization of Dynamically Reconfigurable Embedded Systems," IMEC vzw, 2003, Belgium, 7 pages, <a href="http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf">http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf</a> .
	Miyamori, T. et al., "REMARC: Reconfigurable Multimedia Array Coprocessor," Computer Systems Laboratory, Stanford University, IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS E SERIES D, 1999; (abstract): Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays, p.261, February 22-25, 1998, Monterey, California, United States, pp. 1-12.
	Moraes, F., et al., "A Physical Synthesis Design Flow Based on Virtual Components," XV Conference on Design of Circuits and Integrated Systems (November 2000) 6 pages
	Muchnick, S., "Advanced Compiler Design and Implementation" (Morgan Kaufmann 1997), Table of Contents, 11 pages
	Murphy, C., "Virtual Hardware Using Dynamic Reconfigurable Field Programmable Gate Arrays," Engineering Development Centre, Liverpool John Moores University, UK, GERI Annual Research Symposium 2005, 8 pages.
	Nageltinger, U., "Design-Space Exploration for Coarse Grained Reconfigurable Architectures," (Dissertation) Universitaet Kaiserslautern, 2000, Chapter 2, pp. 19-45.
	Neumann, T., et al., "A Generic Library for Adaptive Computing Environments," Field Programmable Logic and Applications, 11 <sup>th</sup> International Conference, FPL 2001, Proceedings (Lecture Notes in Computer Science, vol. 2147) (2001) pp. 503-512
	Olukotun, K., "The Case for a Single-Chip Microprocessor," ACM Sigplan Notices, ACM, Association for Computing Machinery, New York, Vol. 31, No. 9, September 1996 (1996-09-00) pp. 2-11.
	PACT Corporation, "The XPP Communication System," Technical Report 15 (2000), pp. 1-16.
	Quenot, G.M., et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Laboratoire Systeme de Perception, DGA/Etablissement Technique Central de l'Armement, France, 1994 IEEE, pp. 91-100.

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/96

Serial No.  
10/551891

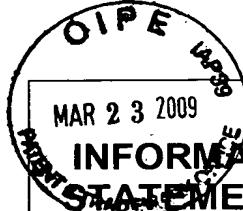
Applicant(s)  
Vorbach et al.

Filing Date  
August 28, 2006

Group Art Unit  
2125

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Parhami, B., "Parallel Counters for Signed Binary Signals," Signals, Systems and Computers, 1989, Twenty-Third Asilomar Conference, Volume 1, pp. 513-516.
	Saleeba, Z.M.G., "A Self-Reconfiguring Computer System," Department of Computer Science, Monash University (Dissertation) 1998, pp. 1-306.
	Schmidt, H. et al., "Behavioral synthesis for FGPA-based computing," Carnegie Mellon University, Pittsburgh, PA, 1994 IEEE, pp. 125-132.
	Schönenfeld, M., et al., "The LISA Design Environment for the Synthesis of Array Processors Including Memories for the Data Transfer and Fault Tolerance by Reconfiguration and Coding Techniques," J. VLSI Signal Processing Systems for Signal, Image, and Video Technology, (1 October 1995) vol. 11(1/2), pp. 51-74
	Shin, D., et al., "C-based Interactive RTL Design Methodology," Technical Report CECS-03-42 (December 2003) pp. 1-16
	Singh, H. et al., "MorphoSys: An Integrated Reconfigurable System for Data-Parallel Computation-Intensive Applications," University of California, Irvine, CA. and Federal University of Rio de Janeiro, Brazil, 2000, IEEE Transactions on Computers, pp. 1-35.
	Sondervan, J., "Retiming and logic synthesis," Electronic Engineering (January 1993) vol. 65(793), pp.33, 35-36
	Soni, M., "VLSI Implementation of a Wormhole Run-time Reconfigurable Processor," June 2001, (Masters Thesis)Virginia Polytechnic Institute and State University, 88 pages.
	Sutton et al., "A Multiprocessor DSP System Using PADDI-2," U.C. Berkeley, 1998 ACM, pp. 62-65.
	Tsutsui, A., et al., "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing," NTT Optical Network Systems Laboratories, Japan, 1997 ACM, pp. 93-99.
	Vasell et al., "The Function Processor: A Data-Driven Processor Array for Irregular Computations," Chalmers University of Technology, Sweden, pp. 1-21
	Waingold, E., et al., "Baring it all to software: Raw machines," IEEE Computer, September 1997, at 86-93
	Weinhardt, Markus et al., "Memory Access Optimization for Reconfigurable Systems," IEEE Proceedings Computers and Digital Techniques, 48(3) (May 2001) pp. 1-16.
	Wolfe, M. et al., "High Performance Compilers for Parallel Computing" (Addison-Wesley 1996) Table of Contents, 11 pages.
	XILINX, "Spartan and SpartanXL Families Field Programmable Gate Arrays," January 1999, Xilinx, pp. 4-3 through 4-70.
	XILINX, "XC6200 Field Programmable Gate Arrays," April 24, 1997, Xilinx product description, pp. 1-73.
	XILINX, "XC3000 Series Field Programmable Gate Arrays," November 6, 1998, Xilinx product description, pp. 1-76.
	XILINX, "XC4000E and XC4000X Series Field Programmable Gate Arrays," May 14, 1999, Xilinx product description, pp. 1-68.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," July 17, 2002, Xilinx Production Product Specification, pp. 1-118.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA User Guide," March 28, 2007, Xilinx user guide, pp. 1-559.
	Zhang, et al., "A 1-V Heterogeneous Reconfigurable DSP IC for Wireless Baseband Digital Signal Processing," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000, pp. 1697-1704.
	Zhang et al., "Abstract: Low-Power Heterogeneous Reconfigurable Digital Signal Processors with Energy-Efficient Interconnect Network," U.C. Berkeley (2004), pp. 1-120.
	Zima, H. et al., "Supercompilers for parallel and vector computers" (Addison-Wesley 1991) Table of Contents, 5 pages.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



MAR 23 2009

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/96Serial No.  
10/551891Applicant(s)  
Vorbach et al.Filing Date  
August 28, 2006Group Art Unit  
2125**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE37,195	May 29, 2001	Kean			
	4,590,583	May 20, 1986	Miller			
	4,667,190	May 1987	Fant et al.			
	4,972,314	November 1990	Getzinger et al.			
	5,010,401	April 1991	Murakami et al.			
	5,034,914	July 1991	Osterlund			
	5,041,924	August 1991	Blackborow et al.			
	5,065,308	November 12, 1991	Evans			
	5,099,447	March 1992	Myszewski			
	5,237,686	August 1993	Asano et al.			
	5,276,836	January 4, 1994	Fukumaru et al.			
	5,327,125	July 1994	Iwase et al.			
	5,343,406	Aug 30, 1994	Freeman et al.			
	5,418,953	May 1995	Hunt et al.			
	5,469,003	November 1995	Kean			
	5,537,580	July 1996	Giomi et al.			
	5,550,782	Aug 27, 1996	Cliff et al.			
	5,625,836	Apr 29, 1997	Barker et al.			
	5,646,544	Jul 8, 1997	Iadanaz			
	5,646,545	Jul 8, 1997	Trimberger et al.			
	5,581,731	December 3, 1996	King et al.			
	5,737,565	April 1998	Mayfield			
	5,754,459	May 19, 1998	Telikepalli			
	5,754,820	May 19, 1998	Yamagami			
	5,781,756	Jul 14, 1998	Hung			
	5,781,756	Jul 14, 1998	Hung			
	5,801,958	September 1998	Dangelo et al.			
	5,815,715	September 1998	Kayhan			
	5,831,448	Nov 3, 1998	Kean			
	5,844,422	December 1, 1998	Trimberger et al.			
	5,857,097	January 1999	Henzinger et al.			
	5,862,403	January 1999	Kanai et al.			
	5,870,620	Feb 9, 1999	Kadosumi et al.			
	5,889,533	Mar 30, 1999	Lee			
	5,933,023	Aug 3, 1999	Young			
	5,960,193	September 28, 1999	Guttag et al.			
	5,966,143	Oct 12, 1999	Breternitz, Jr.			
	5,978,583	November 1999	Ekanadham et al.			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>		Attorney Docket No. <b>2885/96</b>	Serial No. <b>10/551891</b>
		Applicant(s) <b>Vorbach et al.</b>	
Filing Date <b>August 28, 2006</b>		Group Art Unit <b>2125</b>	

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,999,990	December 1999	Sharrit et al.			
	6,020,760	February 1, 2000	Sample et al.			
	6,044,030	Mar 28, 2000	Zheng et al.			
	6,077,315	June 2000	Greenbaum et al.			
	6,084,429	July 2000	Trimberger			
	6,105,106	August 2000	Manning			
	6,134,166	October 17, 2000	Lytle et al.			
	6,137,307	October 2000	Iwanczuk et al.			
	6,154,048	November 2000	Iwanczuk et al.			
	6,154,049	Nov 28, 2000	New			
	6,157,214	December 5, 2000	Marshall			
	6,185,256	February 2001	Saito et al.			
	6,185,731	February 2001	Maeda et al.			
	6,198,304	March 2001	Sasaki			
	6,201,406	March 2001	Iwanczuk et al.			
	6,204,687	March 2001	Schultz et al.			
	6,215,326	April 10, 2001	Jefferson et al.			
	6,216,223	April 2001	Revilla et al.			
	6,252,792	June 26, 2001	Marshall et al.			
	6,262,908	July 17, 2001	Marshall et al.			
	6,266,760	July 2001	DeHon et al.			
	6,285,624	September 2001	Chen			
	6,311,265	October 2001	Beckerle et al.			
	6,353,841	March 5, 2002	Marshall et al.			
	6,362,650	Mar 26, 2002	New et al.			
	6,373,779	Apr 16, 2002	Pang et al.			
	6,381,624	April 2002	Colon-Bonet et al.			
	6,400,601	June 2002	Sudo et al.			
	6,421,808	July 2002	McGeer			
	6,427,156	Jul 30, 2002	Chapman et al.			
	6,430,309	August 2002	Pressman et al.			
	6,434,642	Aug 13, 2002	Camilleri et al.			
	6,438,747	August 2002	Schreiber et al.			
	6,477,643	November 5, 2002	Vorbach et al.			
	6,487,709	November 2002	Keller et al.			
	6,507,947	January 2003	Schreiber et al.			
	6,516,382	February 2003	Manning			
	6,518,787	February 2003	Allegrucci et al.			

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No. 2885/96	Serial No. 10/551891
Applicant(s) Vorbach et al.	
Filing Date August 28, 2006	Group Art Unit 2125

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,523,107	February 18, 2003	Stansfield et al.			
	6,525,678	February 2003	Veenstra et al.			
	6,539,415	March 25, 2003	Mercs			
	6,539,438	March 25, 2003	Ledzius et al.			
	6,542,394	April 1, 2003	Marshall et al.			
	6,553,395	April 22, 2003	Marshall et al.			
	6,567,834	May 20, 2003	Marshall et al.			
	6,631,487	October 2003	Abramovici et al.			
	6,708,325	March 2004	Cooke et al.			
	6,721,830	April 2004	Vorbach et al.			
	6,754,805	June 2004	Yujen Juan			
	6,757,892	June 2004	Gokhale et al.			
	6,782,445	August 2004	Olgiati et al.			
	6,802,206	October 2004	Patterson et al.			
	6,820,188	November 16, 2004	Stansfield et al.			
	6,829,697	December 2004	Davis et al.			
	6,847,370	January 2005	Baldwin et al.			
	6,871,341	March 2005	Shyr			
	6,874,108	March 2005	Abramovici et al.			
	6,977,649	December 2005	Baldwin et al.			
	7,007,096	February 2006	Lisitsa et al.			
	7,010,687	March 2006	Ichimura			
	7,038,952	May 2, 2006	Zack et al.			
	7,210,129	April 2007	May et al.			
	7,237,087	June 26, 2007	Vorbach et al.			
	7,249,351	July 2007	Songer et al.			
	7,254,649	August 2007	Subramanian et al.			
	7,350,178	March 2008	Crosland et al.			
	2001/001860	May 2001	Bieu			
	2002/124238	September 05, 2002	Metzgen			
	2003/061542	March 2003	Bates et al.			
	2003/062922	Apr 3, 2003	Douglass et al.			
	2005/0144210	Jun 30, 2005	Simkins et al.			
	2005/0144212	Jun 30, 2005	Simkins et al.			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. <b>2885/96</b>	Serial No. <b>10/551891</b>
	Applicant(s) <b>Vorbach et al.</b>	
	Filing Date <b>August 28, 2006</b>	Group Art Unit <b>2125</b>

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	2005/0144215	Jun 30, 2005	Simkins et al.			
	2005/066213	March 2005	Vorbach et al.			
	2006/0230094	Oct 12, 2006	Simkins et al.			
	2006/0130096	Oct 12, 2006	Thendean et al.			

#### FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 746 106	December 4, 1996	EPO				
	1 061 439	December 20, 2000	EPO				
	1 669 885	Jun 14, 2006	EPO			Abstract	
	WO98/10517	March 12, 1998	PCT				
	WO98/35294	August 13, 1998	PCT				
	WO00/49496	August 24, 2000	PCT				
	WO02/50665	June 27, 2002	PCT				
	WO 2004/053718	June 24, 2004	PCT				
	WO05/045692	May 19, 2005	PCT				
	05-509184	December 16, 2003	Japan			English Equivalent = USP 5,193,202 cited above	
	08069447	March 12, 1996	Japan			Abstract	
	2001-500682	January 16, 2001	Japan			Abstract	
	2000-201066	July 18, 2000	Japan			Abstract	

#### OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Abnous et al., "Ultra-Low-Power Domain-Specific Multimedia Processors," U.C. Berkeley, 1996 IEEE, pp. 461-470.
	Albharna, O.T. et al., "On the Viability of FPGA-Based Integrated Coprocessors," Dept. of Electrical and Electronic Engineering, Imperial College of Science, London, 1999 IEEE, pp. 206-215.
	Altera, "Flex 8000 Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-62.
	Altera, "Flex 10K Embedded Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-128.
	Atmel, 5-K-50K Gates Coprocessor FPGA with Free Ram, Data Sheet, July 2006, 55 pages.
	Atmel, FPGA-based FIR Filter Application Note, September 1999, 10 pages.
	Atmel, "An Introduction to DSP Applications using the AT40K FPGA," FPGA Application Engineering, San Jose, CA, April 2004, 15 pages.
	Atmel, Configurable Logic Design & Application Book, Atmel Corporation, 1995, pp. 2-19 through 2-25.

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No. 2885/96	Serial No. 10/551891
Applicant(s) Vorbach et al.	
Filing Date August 28, 2006	Group Art Unit 2125

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Atmel, Field Programmable Gate Array Configuration Guide, AT6000 Series Configuration Data Sheet, September 1999, pp. 1-20.
	Athanasiou et al., "Processor Reconfiguration Through Instruction-Set Metamorphosis," 1993, IEEE Computers, pp. 11-18.
	Bakkes, P.J., et al., "Mixing Fixed and Reconfigurable Logic for Array Processing," Dept. of Electrical and Electronic Engineering, University of Stellenbosch, South Africa, 1996 IEEE, pp. 118-125.
	Bacon, D. et al., "Compiler Transformations for High-Performance Computing," ACM Computing Surveys, 26(4):325-420 (1994)
	Becker, J. et al., "Architecture, Memory and Interface Technology Integration of an Industrial/Academic Configurable System-on-Chip (CSoC)," IEEE Computer Society Annual Workshop on VLSI (WVLSI 2003), (February 2003)
	Becker, J., "Configurable Systems-on-Chip (CSoC)," (Invited Tutorial), Proc. of 9th Proc. of XV Brazilian Symposium on Integrated Circuit, Design (SBCCI 2002), (September 2002)
	Becker et al., "Automatic Parallelism Exploitation for FPL-Based Accelerators." 1998, Proc. 31 <sup>st</sup> Annual Hawaii International Conference on System Sciences, pp. 169-178.
	Bratt, A., "Motorola field programmable analogue arrays, present hardware and future trends," Motorola Programmable Technology Centre, Gadbrook Business Centre, Northwich, Cheshire, 1998, The Institute of Electrical Engineers, IEE. Savoy Place, London, pp. 1-5.
	Cardoso, J.M.P. et al., "A novel algorithm combining temporal partitioning and sharing of functional units," University of Algarve, Faro, Portugal, 2001 IEEE, pp. 1-10.
	Cardoso, J.M.P. et al., "Compilation and Temporal Partitioning for a Coarse-Grain Reconfigurable Architecture," LYSACHT, P. & ROSENTIEL, W. eds., "New Algorithms, Architectures and Applications for Reconfigurable Computing," (2005) pp. 105-115
	Cardoso, J.M.P. et al., "Macro-Based Hardware Compilation of Java <sup>TM</sup> Bytecodes into a Dynamic Reconfigurable Computing System," Field-Programmable Custom Computing Machines (1999) FCCM '99. Proceedings. Seventh Annual IEEE Symposium on NAPA Valley, CA, USA, 21-23 April 1999, IEEE Comput. Soc, US, (21 April 1999) pp.2-11
	Compton, K. et al., "Configurable Computing: A Survey of Systems and Software," Northwestern University, Dept. of ECE, Technical Report, 1999, (XP-002315148), 39 pages.
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0702, 2007, pp. 1-15, <a href="http://www.clearspeed.com">www.clearspeed.com</a> .
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0306, 2006, pp. 1-14, <a href="http://www.clearspeed.com">www.clearspeed.com</a> .
	Cook, Jeffrey J., "The Amalgam Compiler Infrastructure," Thesis at the University of Illinois at Urbana-Champaign (2004) Chapter 7 & Appendix G
	Cronquist, D. et al., "Architecture Design of Reconfigurable Pipelined Datapaths," Department of Computer Science and Engineering, University of Washington, Seattle, WA, Proceedings of the 20 <sup>th</sup> Anniversary Conference on Advanced Research in VSLI, 1999, pp. 1-15.
	DeHon, Andre, "Reconfigurable Architectures for General-Purpose Computing," Massachusetts Institute of Technology, Technical Report AIRTR-1586, October 1996 (1996-10), XP002445054, Cambridge, MA, pp. 1-353.
	Diniz, P., et al., "A behavioral synthesis estimation interface for configurable computing," University of Southern California, Marina Del Rey, CA, 2001 IEEE, pp. 1-2.
	Ebeling, C. et al., "Mapping Applications to the RaPiD Configurable Architecture," Department of Computer Science and Engineering, University of Washington, Seattle, WA, FPGAs for Custom Computing Machines, 1997. Proceedings., The 5th Annual IEEE Symposium, Publication Date: 16-18 Apr 1997, 10 pages.
	Equator, Pixels to Packets, Enabling Multi-Format High Definition Video, Equator Technologies BSP-15 Product Brief, <a href="http://www.equator.com">www.equator.com</a> , 2001, 4 pages.
	Fawcett, B.K., "Map, Place and Route: The Key to High-Density PLD Implementation," Wescon Conference, IEEE Center (7 November 1995) pp. 292-297
	Freescale Slide Presentation, An Introduction to Motorola's RCF (Reconfigurable Compute Fabric) Technology, Presented by Frank David, Launched by Freescale Semiconductor, Inc., 2004, 39 pages.
	Genius, D. et al., "A Case for Array Merging in Memory Hierarchies," Proceedings of the 9th International Workshop on Compilers for Parallel Computers, CPC'01 (June 2001), 10 pages.
	Hartenstein, R. et al., "A new FPGA architecture for word-oriented datapaths," Proc. FPL'94, Springer LNCS, September 1994, pp. 144-155.
	Hendrich, N., et al., "Silicon Compilation and Rapid Prototyping of Microprogrammed VLSI-Circuits with MIMOLA and SOLO 1400," Microprocessing & Microprogramming (September 1992) vol.35(1-5), pp. 287-294

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/96

Serial No.  
10/551891

Applicant(s)  
Vorbach et al.

Filing Date  
August 28, 2006

Group Art Unit  
2125

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Hwang, K., "Advanced Computer Architecture – Parallelism, Scalability, Programmability," 1993, McGraw-Hill, Inc., pp. 348-355.
	Hwang, K., "Computer Architecture and Parallel Processing," Data Flow Computers and VLSI Computations, XP-002418655, 1985 McGraw-Hill, Chapter 10, pp. 732-807.
	IBM Technical Disclosure Bulletin, IBM Corp., New York, XP000424878, Bd. 36, Nr. 11, 1 November 1993, pp. 335-336.
	Inside DSP, "Ambric Discloses Massively Parallel Architecture," August 23, 2006, <a href="HTTP://insidedsp.com/tabid/64/articleType/ArticleView/articleId/155/Defa...">HTTP://insidedsp.com/tabid/64/articleType/ArticleView/articleId/155/Defa...</a> , 2 pages.
	Intel, Intel MXP5800/MXP5400 Digital Media Processors, Architecture Overview, June 2004, Revision 2.4, pp. 1-14.
	Kaul, M., et al., "An automated temporal partitioning and loop fission approach of FPGA based reconfigurable synthesis of DSP applications," University of Cincinnati, Cincinnati, OH, ACM 1999, pp. 616-622.
	Kean, T.A., "Configurable Logic: A Dynamically Programmable Cellular Architecture and its VLSI Implementation," University of Edinburgh (Dissertation) 1988, pp. 1-286
	Kean, T., et al., "A Fast Constant Coefficient Multiplier for the XC6200," Xilinx, Inc., Lecture Notes in Computer Science, Vol. 1142, Proceedings of the 6 <sup>th</sup> International Workshop of Field-Programmable Logic, 1996, 7 pages.
	Kim et al., "A Reconfigurable Multifunction Computing Cache Architecture," IEEE Transactions on Very Large Scale Integration (VLSI) Systems Volume 9, Issue 4, Aug 2001 Page(s):509 – 523.
	Knittel, Gunter, "A PCI-compatible FPGA-Coprocessor for 2D/3D Image Processing," University of Turgingen, Germany, 1996 IEEE, pp. 136-145.
	Koch, Andreas et al., "High-Level-Language Compilation for Reconfigurable Computers," Proceedings of European Workshop on Reconfigurable Communication-Centric SOCS (June 2005) 8 pages
	Larsen, S. et al., "Increasing and Detecting Memory Address Congruence," Proceedings of the 2002 IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'02), pp. 1-12 (September 2002).
	Lee et al., "A new distribution network based on controlled switching elements and its applications," IEEE/ACT Trans. of Networking, Vol. 3, No. 1, pp. 70-81, February 1995.
	Margolus, N., "An FPGA architecture for DRAM-based systolic computations," Boston University Center for Computational Science and MIT Artificial Intelligence Laboratory, IEEE 1997, pp. 2-11.
	Mei, Bingfeng, "A Coarse-Grained Reconfigurable Architecture Template and Its Compilation Techniques," Katholieke Universiteit Leuven, PhD Thesis, January 2005, IMEC vzw, Universitair Micro-Electronica Centrum, Belgium, pp. 1-195 (and Table of Contents).
	Mei, Bingfeng, et al., "Design and Optimization of Dynamically Reconfigurable Embedded Systems," IMEC vzw, 2003, Belgium, 7 pages, <a href="http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf">http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf</a> .
	Miyamori, T. et al., "REMARC: Reconfigurable Multimedia Array Coprocessor," Computer Systems Laboratory, Stanford University, IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS E SERIES D, 1999; (abstract): Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays, p.261, February 22-25, 1998, Monterey, California, United States, pp. 1-12.
	Moraes, F., et al., "A Physical Synthesis Design Flow Based on Virtual Components," XV Conference on Design of Circuits and Integrated Systems (November 2000) 6 pages
	Muchnick, S., "Advanced Compiler Design and Implementation" (Morgan Kaufmann 1997), Table of Contents, 11 pages
	Murphy, C., "Virtual Hardware Using Dynamic Reconfigurable Field Programmable Gate Arrays," Engineering Development Centre, Liverpool John Moores University, UK, GERI Annual Research Symposium 2005, 8 pages.
	Nagelddinger, U., "Design-Space Exploration for Coarse Grained Reconfigurable Architectures," (Dissertation) Universitaet Kaiserslautern, 2000, Chapter 2, pp. 19-45.
	Neumann, T., et al., "A Generic Library for Adaptive Computing Environments," Field Programmable Logic and Applications, 11 <sup>th</sup> International Conference, FPL 2001, Proceedings (Lecture Notes in Computer Science, vol. 2147) (2001) pp. 503-512
	Olukotun, K., "The Case for a Single-Chip Microprocessor," ACM Sigplan Notices, ACM, Association for Computing Machinery, New York, Vol. 31, No. 9, September 1996 (1996-09-00) pp. 2-11.
	PACT Corporation, "The XPP Communication System," Technical Report 15 (2000), pp. 1-16.
	Quenot, G.M., et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Laboratoire Systeme de Perception, DGA/Etablissement Technique Central de l'Armement, France, 1994 IEEE, pp. 91-100.

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No. 2885/96	Serial No. 10/551891
Applicant(s) <b>Vorbach et al.</b>	
Filing Date <b>August 28, 2006</b>	Group Art Unit <b>2125</b>

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Parhami, B., "Parallel Counters for Signed Binary Signals," Signals, Systems and Computers, 1989, Twenty-Third Asilomar Conference, Volume 1, pp. 513-516.
	Saleeba, Z.M.G., "A Self-Reconfiguring Computer System," Department of Computer Science, Monash University (Dissertation) 1998, pp. 1-306.
	Schmidt, H. et al., "Behavioral synthesis for FGPA-based computing," Carnegie Mellon University, Pittsburgh, PA, 1994 IEEE, pp. 125-132.
	Schönfeld, M., et al., "The LISA Design Environment for the Synthesis of Array Processors Including Memories for the Data Transfer and Fault Tolerance by Reconfiguration and Coding Techniques," J. VLSI Signal Processing Systems for Signal, Image, and Video Technology, (1 October 1995) vol. 11(1/2), pp. 51-74
	Shin, D., et al., "C-based Interactive RTL Design Methodology," Technical Report CECS-03-42 (December 2003) pp. 1-16
	Singh, H. et al., "MorphoSys: An Integrated Reconfigurable System for Data-Parallel Computation-Intensive Applications," University of California, Irvine, CA. and Federal University of Rio de Janeiro, Brazil, 2000, IEEE Transactions on Computers, pp. 1-35.
	Sondervan, J., "Retiming and logic synthesis," Electronic Engineering (January 1993) vol. 65(793), pp.33, 35-36
	Soni, M., "VLSI Implementation of a Wormhole Run-time Reconfigurable Processor," June 2001, (Masters Thesis)Virginia Polytechnic Institute and State University, 88 pages.
	Sutton et al., "A Multiprocessor DSP System Using PADDI-2," U.C. Berkeley, 1998 ACM, pp. 62-65.
	Tsutsui, A., et al., "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing," NTT Optical Network Systems Laboratories, Japan, 1997 ACM, pp. 93-99.
	Vasell et al., "The Function Processor: A Data-Driven Processor Array for Irregular Computations," Chalmers University of Technology, Sweden, pp. 1-21
	Waingold, E., et al., "Baring it all to software: Raw machines," IEEE Computer, September 1997, at 86-93
	Weinhardt, Markus et al., "Memory Access Optimization for Reconfigurable Systems," IEEE Proceedings Computers and Digital Techniques, 48(3) (May 2001) pp. 1-16.
	Wolfe, M. et al., "High Performance Compilers for Parallel Computing" (Addison-Wesley 1996) Table of Contents, 11 pages.
	XILINX, "Spartan and SpartanXL Families Field Programmable Gate Arrays," January 1999, Xilinx, pp. 4-3 through 4-70.
	XILINX, "XC6200 Field Programmable Gate Arrays," April 24, 1997, Xilinx product description, pp. 1-73.
	XILINX, "XC3000 Series Field Programmable Gate Arrays," November 6, 1998, Xilinx product description, pp. 1-76.
	XILINX, "XC4000E and XC4000X Series Field Programmable Gate Arrays," May 14, 1999, Xilinx product description, pp. 1-68.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," July 17, 2002, Xilinx Production Product Specification, pp. 1-118.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA User Guide," March 28, 2007, Xilinx user guide, pp. 1-559.
	Zhang, et al., "A 1-V Heterogeneous Reconfigurable DSP IC for Wireless Baseband Digital Signal Processing," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000, pp. 1697-1704.
	Zhang et al., "Abstract: Low-Power Heterogeneous Reconfigurable Digital Signal Processors with Energy-Efficient Interconnect Network," U.C. Berkeley (2004), pp. 1-120.
	Zima, H. et al., "Supercompilers for parallel and vector computers" (Addison-Wesley 1991) Table of Contents, 5 pages.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	